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John F Kacvinsky
Blakely Sokoloff Taylor & Zafman LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

| EXAMINER | |
|---|---|
| MATTIS, JASON E | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/004,765 | SAXENA, RAHUL | |
| | Examiner | Art Unit | |
| | Jason E. Mattis | 2665 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-14,16-21 and 23-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-14,16-21 and 23-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This Office Action is in response to the amendment filed 1/5/06. Due to the amendment, the previous objection to claim 6 has been withdrawn. Claims 2, 15, and 22 have been cancelled. Claims 1, 3-14, 16-21, and 23-33 are currently pending in the application.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 7, and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Aiki et al. (U.S. Pat. 5410540).

**With respect to claim 1**, Aiki et al. discloses a switching apparatus **(See column 3 lines 45-57 and Figure 1 of Aiki et al. for reference to switch 1, which is a switching apparatus)**. Aiki et al. also discloses a first port coupled to receive an input data frame **(See column 3 lines 45-57 and Figure 1 of Aiki et al. for reference to input ports L01 to L0N that receive cells, which are data frames)**. Aiki et al. further discloses a first logic circuit coupled to receive the frame from the first port and configured to determine a number of copies of the input data frame to make and to

make the number of copies **(See column 4 lines 12-39 and Figure 1 of Aiki et al. for reference to cell copy section 3, which is part of a logic circuit that is coupled to receive an input frame and configured to determine a number of copies of the cell to produce and to produce the copies)**. Aiki et al. also discloses a first memory coupled to the first logic circuit and configured to store and read the copies **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to buffer memory 4, which is coupled to the cell copy section 3, and is configured to store and read the cell copies)**. Aiki et al. further discloses a second logic circuit coupled to the first memory and configured to determine when to read at least one copy of the input data frame from the first memory **(See column 5 lines 7-20 and Figure 1 of Aiki et al. for reference to buffer memory controller 6, which is a second logic circuit coupled to buffer memory 4, configured to determine when to read a copy from the buffer memory 4)**. Aiki et al. also discloses a second port coupled to the first memory and configured to transmit the at least one copy of the frame **(See column 5 liens 7-20 and Figure 1 of Aiki et al. for reference to output ports L91 to L9N, which are coupled to the buffer memory 4, configured to transmit read copies of the cell)**. Aiki et al. further discloses that the first logic circuit comprises a third logic circuit configured to determine one or more empty locations in the first memory to store the copies of the input data frame **(See column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to the buffer memory control section 6, which is a third logic circuit that is part of the ATM switch 1, that determines idle addresses, which are addresses of empty locations**

**of the shared buffer memory 4, and stores the idle addresses in an idle address FIFO buffer 64 and for reference using the idle addresses as addresses to store copies of input ATM cells).**

**With respect to claim 3**, Aiki et al. discloses a second memory configured to keep track of all the empty locations in the first memory **(See column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to idle address FIFO buffer 64, which is a second memory stores addresses of empty locations in the buffer memory 4).**

**With respect to claim 7**, Aiki et al. discloses a third logic circuit configured to determine how many additional ports will output copies of the frame and to calculate the amount of storage space needed to store the copies **(See column 4 lines 12-39 and Figure 1 of Aiki et al. for reference to cell copy section 3 containing copy information table 34, which is used to determine the number of copies of the cell to make, and therefore determine the amount of space needed to store the determined number of copies).**

**With respect to claim 11**, Aiki et al. discloses a bus coupled with the first memory and the second port to transmit data including the copy from the memory to the second port **(See Figure 1 of Aiki et al. for reference to a bus L4 connecting the buffer memory 4 with the output ports L91 to L9N such that data is transmitted on the bus L4 from the memory 4 to the ports L91 to L9N).**

**With respect to claim 12**, Aiki et al. discloses a third logic circuit configured to select at least one copy from the bus **(See column 5 lines 7-20 and Figure 1 of Aiki et**

**al. for reference to output select decoder 65, which is a third logic circuit, configured to select an copy of data to output on the bus to the output port)**.

**With respect to claim 13**, Aiki et al. discloses that the second logic circuit is configured to indicate a location in the first memory where the second port is to obtain the frame **(See column 5 lines 7-20 and Figure 1 of Aiki et al. for reference to buffer control section 6 including logic configured to determine where in the buffer memory 4 the data to be output to an output port is stored)**.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-6, 14, and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiki et al. in view of Brahmbhatt (U.S. Pat. 5646886).

**With respect to claim 14**, Aiki et al. discloses a switching apparatus **(See column 3 lines 45-57 and Figure 1 of Aiki et al. for reference to switch 1, which is a switching apparatus)**. Aiki et al. also discloses a first logic circuit coupled to receive the frame and configured to determine a number of copies of the input data frame to make and to make the number of copies **(See column 4 lines 12-39 and Figure 1 of**

**Aiki et al. for reference to cell copy section 3, which is part of a logic circuit that is coupled to receive an input frame and configured to determine a number of copies of the cell to produce and to produce the copies)**. Aiki et al. further discloses a memory coupled to the first logic circuit and configured to store and read the copies **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to buffer memory 4, which is coupled to the cell copy section 3, and is configured to store and read the cell copies)**. Aiki et al. also discloses a second logic circuit coupled to the first memory and configured to determine when to read at least one copy of the input data frame from the first memory **(See column 5 lines 7-20 and Figure 1 of Aiki et al. for reference to buffer memory controller 6, which is a second logic circuit coupled to buffer memory 4, configured to determine when to read a copy from the buffer memory 4)**. Aiki et al. further discloses that the first logic circuit comprises a third logic circuit configured to determine one or more empty locations in the memory to store the copies of the input data frame **(See column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to the buffer memory control section 6, which is a third logic circuit that is part of the ATM switch 1, that determines idle addresses, which are addresses of empty locations of the shared buffer memory 4, and stores the idle addresses in an idle address FIFO buffer 64 and for reference using the idle addresses as addresses to store copies of input ATM cells)**. Aiki et al. does not disclose that the memory is comprised of channels and segments.

**With respect to claims 4-5 and 16-17**, Aiki et al. discloses a third logic circuit determining where there are empty memory locations **(See column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to the control section 6 having logic to determine an empty location in the buffer memory 4 by using buffer 64)**. Aiki et al. does not disclose that the empty memory locations are channels or segments.

**With respect to claim 6**, Aiki et al. does not disclose independently addressable segments that include independently addressable channels.

**With respect to claims 4-6, 14, and 16-17**, Brahmbhatt, in the field of communications, discloses a memory comprised of independently address segments including independently addressable channels **(See column 7 line 37 to column 8 line 26 and Figure 5 of Brahmbhatt for reference to a memory array comprised of independently addressable segments 1-N each including independently addressable rows, which are channels)**. Using a memory comprised of independently address segments including independently addressable channels has the advantage of providing more efficient memory management.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Brahmbhatt, to combine using a memory comprised of independently address segments including independently addressable channels, as suggested by Brahmbhatt, with the system and method of Aiki et al., with the motivation being to provide more efficient memory management.

**With respect to claim 18**, Aiki et al. discloses a third logic circuit configured to determine how many additional ports will output copies of the frame and to calculate the amount of storage space needed to store the copies **(See column 4 lines 12-39 and Figure 1 of Aiki et al. for reference to cell copy section 3 containing copy information table 34, which is used to determine the number of copies of the cell to make, and therefore determine the amount of space needed to store the determined number of copies)**.

6. Claims 8-9 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiki et al. in view of Brahmbhatt as applied to claims 4-6 and 14-18 above, and further in view of Sun et al.

**With respect to claims 8 and 19**, the combination of Aiki et al. and Brahmbhatt does not disclose determining the size of the frame and calculating the space necessary for storage.

**With respect to claims 9 and 20**, the combination of Aiki et al. and Brahmbhatt does not disclose determining how many addressable locations are needed to store the copies of the frame.

**With respect to claims 8-9 and 19-20**, Sun et al., in the field of communications, discloses determining the size of a date frame and determining how many address locations are needed for the frame **(See column 4 lines 58-64, column 6 line 64 to column 7 line 30 and Figures 2, 3A, and 3B of Sun et al. for reference to receiving variable length packets and determining how much storage is**

**needed for the packets based on the size of the packets)**. Determining the size of a date frame and determining how many address locations are needed for the frame has the advantage of allowing the size of data frames to be variable and providing more flexibility in the amount of data transmitted.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Sun et al., to combine determining the size of a date frame and determining how many address locations are needed for the frame, as suggested by Sun et al., with the system and method of Aiki et al. and Brahmbhatt, with the motivation being to allow the size of data frames to be variable and to provide more flexibility in the amount of data transmitted.

7. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Aiki et al. in view of Medina et al. (U.S. Publication US 2005/0041579 A1).

**With respect to claim 10**, Aiki et al. does not disclose that the memory is distributed across the switch.

**With respect to claim 10**, Medina et al., in the field of communications, discloses using a distributed memory in a switch **(See page 2 paragraphs 19-21 and Figure 2 of Medina et al. for reference to the memory being distributed with each port having a dedicated output port)**. Using a distributed memory in a switch has the advantage of allowing each output port to have a dedicated amount of memory such that if data congestion occurs at one output port, the memory of the other output ports is not affected.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Medina et al., to combine using a distributed memory in a switch, as suggested by Medina et al., with the system and method of Aiki et al., with the motivation being to allow allowing each output port to have a dedicated amount of memory such that if data congestion occurs at one output port, the memory of the other output ports is not affected.

8. Claims 21, 26, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiki et al. in view of Moy-Yee et al. (U.S. Pat. 6724761).

**With respect to claim 21**, Aiki et al. discloses a switching apparatus **(See column 3 lines 45-57 and Figure 1 of Aiki et al. for reference to switch 1, which is a switching apparatus)**. Aiki et al. also discloses a first port coupled to receive an input data frame **(See column 3 lines 45-57 and Figure 1 of Aiki et al. for reference to input ports L01 to L0N that receive cells, which are data frames)**. Aiki et al. further discloses a memory coupled to the first logic circuit and configured to store and read the copies **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to buffer memory 4, which is coupled to the cell copy section 3, and is configured to store and read the cell copies)**. Aiki et al. also discloses a logic circuit coupled to receive the frame from the first port and configured to determine a number of copies of the input data frame to make and to make the number of copies **(See column 4 lines 12-39 and Figure 1 of Aiki et al. for reference to cell copy section 3, which is a logic circuit that is coupled to receive an input frame and**

**configured to determine a number of copies of the cell to produce and to produce the copies)**. Aiki et al. further discloses a logic circuit coupled to the first memory and configured to determine when to read at least one copy of the input data frame from the first memory **(See column 5 lines 7-20 and Figure 1 of Aiki et al. for reference to buffer memory controller 6, which is a logic circuit coupled to buffer memory 4, configured to determine when to read a copy from the buffer memory 4)**. Aiki et al. also discloses a second port coupled to the first memory and configured to transmit the at least one copy of the frame **(See column 5 liens 7-20 and Figure 1 of Aiki et al. for reference to output ports L91 to L9N, which are coupled to the buffer memory 4, configured to transmit read copies of the cell)**. Aiki et al. further discloses a third logic circuit configured to determine one or more empty locations in the memory to store the copies of the input data frame **(See column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to the buffer memory control section 6, which is a third logic circuit that is part of the ATM switch 1, that determines idle addresses, which are addresses of empty locations of the shared buffer memory 4, and stores the idle addresses in an idle address FIFO buffer 64 and for reference using the idle addresses as addresses to store copies of input ATM cells)**. Aiki et al. does not disclose that the logic circuits are embodied as a processor.

**With respect to claim 29**, Aiki et al. discloses a switching apparatus **(See column 3 lines 45-57 and Figure 1 of Aiki et al. for reference to switch 1, which is a switching apparatus)**. Aiki et al. also discloses determining a number of copies of

the input data frame to make and generating the number of copies **(See column 4 lines 12-39 and Figure 1 of Aiki et al. for reference to cell copy section 3, which is a logic circuit that is coupled to receive an input frame and configured to determine a number of copies of the cell to produce and to produce the copies)**. Aiki et al. further discloses determining one or more empty locations in the memory **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to the control section 6 having logic to determine an empty location in the buffer memory 4 by using buffer 64)**. Aiki et al. also discloses forwarding instructions and data to the memory to store the copies in the memory **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to buffer memory 4, which is coupled to the cell copy section 3, and is configured to store copies based on instructions)**. Aiki et al. further discloses forwarding instructions to the memory to read out at least one copy of the input data frame from the first memory **(See column 5 lines 7-20 and Figure 1 of Aiki et al. for reference to buffer memory controller 6, which is a second logic circuit coupled to buffer memory 4, configured to determine when to read a copy from the buffer memory 4)**. Aiki et al. also discloses forwarding instructions to a port causing it to receive and to transmit the at least one copy of the frame **(See column 5 liens 7-20 and Figure 1 of Aiki et al. for reference to output ports L91 to L9N, which are coupled to the buffer memory 4, configured to transmit read copies of the cell)**. Aiki et al. further discloses determining one or more empty locations in the memory to store the copies of the input data frame **(See column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and Figure 1 of**

**Aiki et al. for reference to the buffer memory control section 6, which is a third logic circuit that is part of the ATM switch 1, that determines idle addresses, which are addresses of empty locations of the shared buffer memory 4, and stores the idle addresses in an idle address FIFO buffer 64 and for reference using the idle addresses as addresses to store copies of input ATM cells)**. Aiki et al. does not disclose that the instructions are stored on a computer readable medium and executed by a processor.

**With respect to claims 21 and 29**, Moy-Yee et al. discloses using a microprocessor and software on a computer readable medium to store and execute instructions for operating a switching apparatus **(See column 5 lines 44-51 of Moy-Yee et al. for reference to using a microprocessor and software)**. Using a microprocessor and software on a computer readable medium to store and execute instructions for operating a switching apparatus has the advantage of allowing the system instructions to be written in software such that it is easy to reconfigure new instructions without changing the hardwiring of the apparatus.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Moy-Yee et al., to combine using a microprocessor and software on a computer readable medium to store and execute instructions for operating a switching apparatus with the system and method of Aiki et al., with the motivation being to allow the system instructions to be written in software such that it is easy to reconfigure new instructions without changing the hardwiring of the apparatus.

**With respect to claim 26**, Aiki et al. discloses a determining how many additional ports will output copies of the frame and to calculate the amount of storage space needed to store the copies **(See column 4 lines 12-39 and Figure 1 of Aiki et al. for reference to cell copy section 3 containing copy information table 34, which is used to determine the number of copies of the cell to make, and therefore determine the amount of space needed to store the determined number of copies)**.

9. Claims 23-25 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiki et al. in view of Moy-Yee et al. as applied to claims 21-22, 26, and 29 above, and further in view of Brahmbhatt.

**With respect to claims 23-24 and 30**, Aiki et al. discloses a third logic circuit determining where there are empty memory locations **(See column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to the control section 6 having logic to determine an empty location in the buffer memory 4 by using buffer 64)**. The combination of Aiki et al. and Moy-Yee et al. does not disclose that the empty memory locations are channels or segments.

**With respect to claim 25**, the combination of Aiki et al. and Moy-Yee et al. does not disclose independently addressable segments that include independently addressable channels.

**With respect to claim 31**, the combination of Aiki et al. and Moy-Yee et al. does not disclose storing the copies in multiple segments.

**With respect to claim 32**, the combination of Aiki et al. and Moy-Yee et al. does not disclose that when the memory reads out one copy, the memory also reads out a previously stored copy of a previously received frame.

**With respect to claims 23-25, and 30-32**, Brahmbhatt, in the field of communications, discloses a memory comprised of independently address segments including independently addressable channels **(See column 7 line 37 to column 8 line 26 and Figure 5 of Brahmbhatt for reference to a memory array comprised of independently addressable segments 1-N each including independently addressable rows, which are channels, with the memories of different segments being accessible a the same time)**. Using a memory comprised of independently address segments including independently addressable channels has the advantage of providing more efficient memory management.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Brahmbhatt, to combine using a memory comprised of independently address segments including independently addressable channels, as suggested by Brahmbhatt, with the system and method of the combination of Aiki et al. and Moy-Yee et al., with the motivation being to provide more efficient memory management.

10. Claims 27-28 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aiki et al. in view of Moy-Yee et al. as applied to claims 21-22, 26, and 29 above, and further in view of Sun et al.

**With respect to claim 27**, the combination of Aiki et al. and Moy-Yee et al. does not disclose determining the size of the frame and calculating the space necessary for storage.

**With respect to claim 28**, the combination of Aiki et al. and Moy-Yee et al. does not disclose determining how many addressable locations are needed to store the copies of the frame.

**With respect to claim 33**, the combination of Aiki et al. and Moy-Yee et al. does not disclose determining the size of received data and determining where to store the received data.

**With respect to claims 27-28 and 33**, Sun et al., in the field of communications, discloses determining the size of a date frame and determining how many address locations are needed for the frame **(See column 4 lines 58-64, column 6 line 64 to column 7 line 30 and Figures 2, 3A, and 3B of Sun et al. for reference to receiving variable length packets and determining how much storage is needed for the packets based on the size of the packets)**. Determining the size of a date frame and determining how many address locations are needed for the frame has the advantage of allowing the size of data frames to be variable and providing more flexibility in the amount of data transmitted.

It would have been obvious for one of ordinary skill in the art at the time of the invention, when presented with the work of Sun et al., to combine determining the size of a date frame and determining how many address locations are needed for the frame, as suggested by Sun et al., with the system and method of Aiki et al. and Moy-Yee et

al., with the motivation being to allow the size of data frames to be variable and to provide more flexibility in the amount of data transmitted.

### *Response to Arguments*

11. Applicant's arguments filed 1/5/06 have been fully considered but they are not persuasive.

In response to the argument that:

> "Nowhere...does Aiki disclose determining one or more empty locations in the first memory to store the copies of the input data frame." (See page 12 of Applicant's Remarks section)

the Examiner respectfully disagrees. As shown in the rejections above, Aiki et al. discloses the use of an idle address FIFO buffer 64, which is used to store addresses that are determined to be idle, or empty (See column 3 line 66 to column 4 line 12, column 4 line 58 to column 5 line 6 and Figure 1 of Aiki et al. for reference to the idle address FIFO buffer 64). Since the addresses stored in the buffer 64 have been determined to be idle, and since these addresses are used to store copies of the input data frame, Aiki et al. does disclose determining one or more empty locations in the first memory to store the copies of the input data frame as claimed.

In response to the argument that Aiki et al. does not disclose that the first logic circuit comprises a third logic circuit (See page 13 of Applicant's Remarks section), the Examiner respectfully disagrees. Aiki et al. discloses an ATM switch 1 that, as a whole,

contains many different circuitry elements. The entire circuitry of the ATM switch one is considered to be equivalent to the claimed "first logic circuit". Since the control section 6 is a logic circuit that is part of the circuitry of the ATM switch 1, the control section 6 is a third logic circuit that is part of the first logic circuit of the ATM switch 1 (See Figure 1 of Aiki et al.). Therefore, Aiki et al. does disclose a third logic circuit that is part of the first logic circuit.

## *Conclusion*

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason E. Mattis whose telephone number is (571) 272-3154. The examiner can normally be reached on M-F 8AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jem

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600